

What is claimed is:

1 1. A method of fabricating a semiconductor
2 structure with partially etched gate, comprising the
3 steps of:

4 providing a semiconductor substrate with at least
5 two adjacent gate structures thereon, wherein
6 each gate structure is composed of a gate
7 dielectric layer, a gate conductive layer, a
8 cap layer, sequentially stacked on the
9 substrate, and a lining layer covered on
10 sidewalls thereof;

11 sequentially forming a protective layer and a
12 masking layer over the gate structures;

13 forming an opening in the masking layer and etching
14 the protective layer thereunder to partially
15 expose the lining layer covering one sidewall
16 of the two adjacent gate structures;

17 removing the exposed lining layers;

18 removing the masking layer and the protective layer;
19 and

20 forming a spacer overlying sidewalls of each gate
21 structure to form a plurality of single-side
22 partially etched gate structures.

1 2. The method as claimed in claim 1, further
2 comprising, after removing the exposed lining layers, the
3 step of partially removing the gate conductive layer
4 adjacent to the exposed lining layer.

1 3. The method as claimed in claim 1, further
2 comprising the steps of:

3 forming an inter-layer dielectric layer over the
4 gate structures; and

5 performing photolithography and etching to form a
6 bitline contact in the inter-layer dielectric
7 layer and exposing the substrate and portions
8 of the adjacent gate structures therein.

1 4. The method as claimed in claim 1, wherein the
2 gate conductive layer is composed of a polysilicon layer
3 and a metal silicide layer.

1 5. The method as claimed in claim 4, wherein
2 material of the metal silicide layer is tungsten
3 silicide.

1 6. The method as claimed in claim 1, wherein the
2 protective layer is an anti-reflection coating (ARC)
3 layer.

1 7. The method as claimed in claim 1, wherein
2 material of the masking layer is photoresist (PR).

1 8. The method as claimed in claim 1, wherein
2 materials of the cap layer and the spacer are silicon
3 nitride.

1 9. The method as claimed in claim 1, wherein the
2 lining layer is a rapid thermal oxide (RTO) layer.

1 10. The method as claimed in claim 4, wherein the
2 gate structure adjacent to the exposed lining layer is
3 the metal silicide layer.

1 11. The method as claimed in claim 3, wherein the
2 opening is substantially relative to a position of the
3 bitline contact.

1 12. The method as claimed in claim 3, wherein the
2 method for forming the opening and the bitline contact is
3 nanoimprint lithography (NIL) or photolithography.

1 13. The method as claimed in claim 1, wherein the
2 reticle for forming the opening is bitline contact node
3 reticle or bitline contact reticle.

1 14. The method as claimed in claim 1, wherein
2 removal of the exposed lining layer is achieved using
3 diluted hydrofluoric acid (DHF) or buffer of etching
4 (BOE) etchant.

1 15. The method as claimed in claim 2, wherein
2 partial removal of the gate conductive layer is achieved
3 using of RCA1 etchant.

1 16. A semiconductor structure with a partially
2 etched gate, comprising:

3 a semiconductor substrate;

4 a gate dielectric layer, a gate conductive layer and
5 a cap layer, sequentially stacked on the
6 substrate to form a gate structure; and

7 a lining layer disposed on sidewalls of the gate
8 structure, wherein the lining layer disposed on
9 one sidewall of the gate structure is partially
10 etched to expose the adjacent gate structure.

1 17. The semiconductor structure as claimed in claim
2 16, further comprising:

3 an inter-layer dielectric layer covering the gate
4 structure; and

5 a bitline contact formed in the inter-layer
6 dielectric layer, exposing the substrate and a
7 portion of the gate structure therein, wherein
8 the lining layer of the exposed portion of the
9 gate structure is partially removed.

1 18. The semiconductor structure as claimed in claim
2 16, wherein the exposed gate structure is the gate
3 conductive layer.

1 19. The semiconductor structure as claimed in claim
2 18, wherein the gate conductive layer comprises a
3 polysilicon layer and a metal silicide layer.

1 20. The semiconductor structure as claimed in claim
2 19, wherein the exposed gate structure is the metal
3 silicide layer and portions thereof are partially etched.

1 21. The semiconductor structure as claimed in claim
2 16, further comprising a spacer disposed on sidewalls of
3 each gate structure, covering the lining layer.

1 22. The semiconductor structure as claimed in claim
2 16, wherein the lining layer is a rapid thermal oxide
3 (RTO) layer.

1 23. The semiconductor structure as claimed in claim
2 21, wherein material of the spacer is silicon nitride.

1 24. A method of fabricating a semiconductor
2 structure with partially etched gate, comprising the
3 steps of:

4 providing a semiconductor substrate with at least
5 two adjacent gate structures thereon, wherein
6 each gate structure is composed of a gate
7 dielectric layer, a gate conductive layer, a
8 cap layer, sequentially stacked on the
9 substrate, and a lining layer covered on
10 sidewalls thereof;

11 forming a protective layer over the gate structures;
12 etching portions of the protective layer to
13 partially expose the lining layer covering two
14 sidewalls of each gate structure;

15 removing the exposed lining layers;

16 removing the protective layer; and

17 forming a spacer overlying sidewalls of each gate
18 structures to form a plurality of dual-sided
19 partially etched gate structure.

1 25. The method as claimed in claim 24, further
2 comprising, before removing the partially exposed lining
3 layers, the steps of:

4 forming a masking layer over the protective layer;
5 and
6 forming a plurality of masking patterns in the
7 masking layer, respectively covering the
8 protective layer over the gate structures.

1 26. The method as claimed in claim 24, further
2 comprising, after removing the exposed lining layers, the
3 step of partially removing the gate conductive layer
4 adjacent to the exposed lining layers.

1 27. The method as claimed in claim 24, further
2 comprising the steps of:

3 forming an inter-layer dielectric (ILD) layer over
4 the gate structures; and
5 performing photolithography and etching to form a
6 bitline contact in the inter-layer dielectric
7 layer and exposing the substrate and portions
8 of the adjacent gate structures therein.

1 28. The method as claimed in claim 24, wherein the,
2 gate conductive layer is composed of a polysilicon layer
3 and a metal silicide layer.

1 29. The method as claimed in claim 24, wherein
2 materials of the protective layer are an anti-reflection
3 coating (ARC) and photoresist (PR).

1 30. The method as claimed in claim 24, wherein the
2 protective layer is an anti-reflection coating (ARC)
3 layer and the masking layer is a photoresist (PR) layer.

4 31. The method as claimed in claim 24, wherein
5 materials of the cap layer and the spacer are silicon
6 nitride.

1 32. The method as claimed in claim 27, wherein the
2 gate structure adjacent to the exposed lining layer is
3 the metal silicide layer.

1 33. The method as claimed in claim 24, wherein
2 removal of the exposed lining layer is achieved using
3 diluted hydrofluoric acid (DHF) or buffer of etching
4 (BOE) etchant.

1 34. The method as claimed in claim 26, wherein
2 partially removing the gate conductive layer is achieved
3 using RCA1 solution containing ammonium hydroxide (NH₄OH)
4 and hydrogen peroxide (H₂O₂).

1 35. A semiconductor structure with a partially
2 etched gate, comprising:

3 a semiconductor substrate;

4 a gate dielectric layer, a gate conductive layer and
5 a cap layer, sequentially stacked on the
6 substrate to form a gate structure; and

7 a lining layer disposed on sidewalls of the gate
8 structure, wherein the lining layer disposed on
9 two sidewalls of the gate structure is
10 partially etched to expose the adjacent gate
11 structure.

1 36. The semiconductor structure as claimed in claim
2 35, further comprising:

3 an inter-layer dielectric layer covering the gate
4 structure; and
5 a contact formed in the inter-layer dielectric
6 layer, exposing the substrate and a portion of
7 the gate structure therein, wherein the lining
8 layer of the exposed portion of the gate
9 structure is partially removed.

1 37. The semiconductor structure as claimed in claim
2 35, wherein the exposed gate structure is the gate
3 conductive layer.

1 38. The semiconductor structure as claimed in claim
2 37, wherein the gate conductive layer comprises a
3 polysilicon layer and a silicide layer.

1 39. The semiconductor structure as claimed in claim
2 38, wherein the exposed gate structure is the metal
3 silicide layer with partially etched portions.

1 40. The semiconductor structure as claimed in claim
2 35, further comprising a spacer disposed on sidewalls of
3 the gate structure, covering the lining layer.

1 41. The semiconductor structure as claimed in claim
2 35, wherein the lining layer is a rapid thermal oxide
3 (RTO) layer.

1 42. The semiconductor structure as claimed in claim
2 40, wherein material of the spacer is silicon nitride.